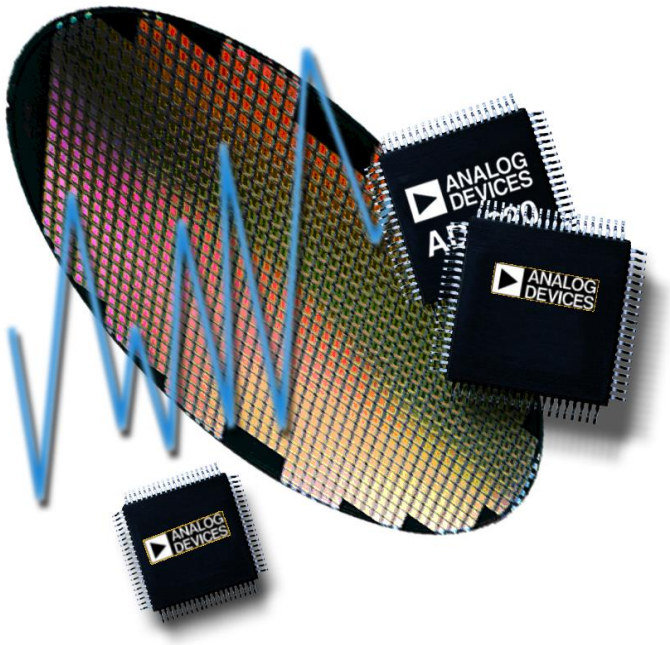

Reliability Report

Report Title: LT8650S Assembly Process Change Automotive Grade 0 Qualification

Report Number: 20616

Revision: A

Date: 26 July 2023

Summary

This report documents the successful completion of the reliability Automotive qualification requirements for the release of the LT8650S product in a 32-LGA package. The LT8650S is a Dual Channel 4A, 42V Synchronous Step-Down Silent Switcher 2.

AECQ100 Qualification Test Methods and Summary

AEC Test Group	AEC Stress Test Name	Abbreviation	AEC Test #	Reference
Group A ACCELERATED ENVIRONMENT STRESS TESTS	Preconditioning	PC	A1	Table 2 and Table 4
	Temperature Humidity Bias or Biased-HAST	THB or HAST	A2	
	Autoclave or Unbiased HAST or Temperature Humidity (without Bias)	AC, UHST, or TH	A3	
	Temperature Cycle	TC	A4	
	Power Temperature Cycling	PTC	A5	
	High Temperature Storage Life	HTSL	A6	
Group B ACCELERATED LIFETIME SIMULATION TESTS	High Temperature Operating Life	HTOL	B1	Table 2 and Table 4
	Early Life Failure Rate	ELFR	B2	
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	
Group C PACKAGE ASSEMBLY INTEGRITY TESTS	Wire Bond Shear	WBS	C1	C1, C2 are only applicable for wire bond package. C5 is only applicable for BGA package. C3, C4 and C6 are qualified and controlled with inline monitors and may be viewed on site at Analog Devices.
	Wire Bond Pull Strength	WBP	C2	
	Solderability	SD	C3	
	Physical Dimensions	PD	C4	
	Solder Ball Shear	SBS	C5	
	Lead Integrity	LI	C6	
Group D DIE FABRICATION RELIABILITY TESTS	Electromigration	EM	D1	Die Fabrication Reliability data may be viewed on-site at Analog Devices.
	Time Dependent Dielectric Breakdown	TDDB	D2	
	Hot Carrier Injection	HCI	D3	
	Negative Bias Temperature Instability	BTI	D4	
	Stress Migration	SM	D5	
Group E ELECTRICAL VERIFICATION TESTS	Pre- and Post-Stress Electrical Test	TEST	E1	Table 5 and Table 6
	Electrostatic Discharge Human Body Model	HBM	E2	
	Electrostatic Discharge Charged Device Model	CDM	E3	
	Latch-Up	LU	E4	
	Electrical Distributions	ED	E5	• For Tests E5, E6 and E7, ADI New Product Yield Analysis Testing Guidelines meet AEC Q100 requirements. • Results for Tests E7-E11 are available as applicable on a case by case basis. • Test E12 results may be viewed on-site at Analog Devices
	Fault Grading	FG	E6	
	Characterization	CHAR	E7	
	Electromagnetic Compatibility	EMC	E9	
	Short Circuit Characterization	SC	E10	
	Soft Error Rate	SER	E11	
	Lead (Pb) Free	LF	E12	
Group F DEFECT SCREENING TESTS	Process Average Test	PAT	F1	ADI New Product Yield Analysis Testing Guidelines meet AECQ100 Requirements.
	Statistical Bin/Yield Analysis	SBA	F2	
Group G CAVITY PACKAGE INTEGRITY TESTS	Mechanical Shock	MS	G1	<Applicable only for Cavity Packages>
	Variable Frequency Vibration	VFV	G2	
	Constant Acceleration	CA	G3	
	Gross/Fine Leak	GFL	G4	
	Package Drop	DROP	G5	
	Lid Torque	LT	G6	
	Die Shear	DS	G7	
	Internal Water Vapor	IWV	G8	

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.35µm DMOS

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data				
Generic/Root Part #	LT8650S	LT8638S	LT8685S	LT8650SP/SPA	LT8648S	LT8686S
Die Id	8650	8638	8685	8650	8648	8686
Die Size (mm)	1.75 x 3.88	2.6x4.0	1.7x4.06	1.75 x 3.88	6.2x2.7	3.2 x 1.75
Wafer Fabrication Site	Vanguard	Vanguard	Vanguard	Vanguard	Vanguard	Vanguard
Wafer Fabrication Process	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS
Metallization / # Layers	AlCu / 3	AlCu / 3	AlCu / 3	AlCu / 3	AlCu / 3	AlCu / 3
Polyimide	No	No	No	No	No	No
Passivation	oxide/SiN	oxide/SiN	oxide/SiN	oxide/SiN	oxide/SiN	oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.35µm DMOS at Vanguard-Taiwan

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Early Life Failure Rate (ELFR)[1]	AEC-Q100-008	Ta=150°C, 48 Hours	LT8650SP	Q17503.1ELFR	0/800
				Z51176.1	0/800
			LT8648S	EO9353.ELFR	0/800
				Z48440.1	0/800
			LT8648SP	Z50105.1	0/800
High Temperature Operating Life (HTOL)[3]	JESD22- A108	Ta=150°C, Biased, 1,000 Hours	LT8686S	Q17405.1BHTOL	0/77
				Q17405.2HTOL	0/77
				Q20395.1HTOL	0/77
			LT8685S	Q17750.1HTOL	0/77
			LT8638S	Q20120.4HTOL	0/77
			LT8650S-1	Q16719.1HTOL	0/77
				Q16719.3HTOL	0/77
			LT8650S	Q20616.3HTOL	0/77
			LT8650SPA	Q20156.1HTOL	0/77
High Temperature Storage Life (HTSL)[1]	JESD22-A103	150°C, 2,000 Hours	LT8648S	EO9353F.HTS	0/45
			LT8686S	Q17405.1HTS	0/45
			LT8650S	20616.3.HTS	0/45
			LT8638S	Q20120.2HTS	0/45
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1,2]	JESD22- A110	130°C 85%RH 33.3 psia, Biased, 192 Hours	LT8648S	EO9237K.BHAST	0/77
		130°C 85%RH 33.3 psia, Biased, 96 Hours	LT8686S	Q17405.1BHAST	0/77
				Q20395.1HAST	0/77
			LT8648S	EO9508K.BHAST	0/77
				EO9353K.BHAST	0/77
			LT8638S	Q20120.1HAST	0/77
				Q20120.3HAST	0/77
			LT8650S	Q20616.4BHAST	0/77
		110°C 85%RH 17.7 psia, Biased, 264 Hours	LT8638S	Q20120.4HAST	0/77

[1] Pre- and post-stress electrical test was performed at room and hot temperatures.
[2] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[3] Electrical test was performed at room, cold and hot temperatures.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 32-LGA at ASE

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data		
Generic/Root Part #	LT8650S	LT8386S	LT8638S	LT8686S
Package	32-LGA	28-LGA	28-LGA	32-LGA
Body Size (mm)	6.00 x 4.00 x 0.94	5x4x0.94	5x4x0.94	5 x 5 x 0.95
Assembly Location	ASE	ASE	ASE	ASE
MSL/Peak Reflow Temperature (°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E
Leadframe Material	BT Resin	BT Resin	BT Resin	BT Resin
Lead Finish	Au	Au	Au	Au
Bumping Foundry	Chipbond	Chipbond	Chipbond	Chipbond
Bumping Process	Electroplating/Cu Pillar	Electroplating/Cu Pillar	Electroplating/Cu Pillar	Electroplating/Cu Pillar
Bump Pitch (mm)	0.165	0.15	0.15	0.13
Bump Diameter (mm)	0.090	0.085	0.085	0.085

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - LGA at ASE (AEK)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
High Temperature Storage Life (HTSL)[1]	JESD22-A103	150°C, 2,000 Hours	LT8638S	Q20120.2HTS	0/45
			LT8686S	Q17405.1HTS	0/45
			LT8650S	Q20616.3HTS	0/45
		175°C, 1,000 Hours	LT8386	Q17381.2HTS	0/45
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1,2]	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 192 Hours	LT8386	Q17381.2BHAST	0/77
				Q17381.3BHAST	0/77
		130°C 85%RH 33.3 psia, Biased, 96 Hours	LT8686S	Q17405.1BHAST	0/77
				Q20395.1HAST	0/77
			LT8638S	Q20120.1HAST	0/77
				Q20120.3HAST	0/77
			LT8650S	Q20616.4HAST	0/77
		110°C 85%RH 17.7psia, Biased, 264 Hours	LT8638S	Q20120.4HAST	0/77
Solder Heat Resistance (SHR)	J-STD-020	MSL-3	LT8650S	Q20616.4SHR	0/77
Temperature Cycling (TC)[1,2]	JESD22-A104	-65°C/+150°C, 2000 Cycles	LT8638S	Q20120.1TC	0/77
				Q20120.2TC	0/77
				Q20120.3TC	0/77
			LT8386	Q17381.2TC	0/77
				Q17381.3TC	0/77
				Q17381.LOT2TC	0/77
			LT8650S	Q20616.4TC	0/77
Unbiased HAST (UHST)[2,3]	JESD22-A118	130°C 85%RH 33.3 psia, 192 Hours	LT8386	Q17381.2UHAST	0/77
				Q17381.3UHAST	0/77
				Q17381.LOT2UHAST	0/77
		130°C 85%RH 33.3 psia, 96 hrs	LT8686S	Q20395.1UHAST	0/77
			LT8650S	Q20616.4AUHAST	0/77
		110°C 85%RH 17.7psia, Biased 264 hrs	LT8638S	Q20120.1UHAST	0/77
				Q20120.3UHAST	0/77

[1] Pre- and post-stress electrical test was performed at room and hot temperatures.
[2] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[3] Electrical test was performed at room temperature.

ESD and Latch-Up Test Results

Table 5: ESD Test Results

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	LT8650S	32-LGA	JS-002	1Ω, Cpkg	±1250V	C3
HBM	LT8650S	32-LGA	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	3A

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Temperature (Ta)	Class
JESD78	LT8650S	-100mA, +100mA	150°C	II

Approvals

Reliability Engineer: Hang Luu